UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|---|---|---|---|---|
| 10/779,808 | 02/18/2004 | Paul Anthony Gilkerson | 550-525 | 6826 |

23117 7590 06/17/2010

NIXON & VANDERHYE, PC
901 NORTH GLEBE ROAD, 11TH FLOOR
ARLINGTON, VA 22203

| EXAMINER | |
|---|---|
| FENNEMA, ROBERT E | |
| **ART UNIT** | **PAPER NUMBER** |
| 2183 | |

| MAIL DATE | DELIVERY MODE |
|---|---|
| 06/17/2010 | PAPER |

**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

UNITED STATES PATENT AND TRADEMARK OFFICE

---

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

---

*Ex parte* PAUL ANTHONY GILKERSON

---

Appeal 2009-013779
Application 10/779,808
Technology Center 2100

---

Decided: June 17, 2010

---

Before LANCE LEONARD BARRY, ST. JOHN COURTENAY III, and JAMES R. HUGHES, *Administrative Patent Judges*.

BARRY, *Administrative Patent Judge*.

## DECISION ON APPEAL

## STATEMENT OF THE CASE

The Patent Examiner rejected claims 1-21. The Appellant appeals therefrom under 35 U.S.C. § 134(a). We have jurisdiction under 35 U.S.C. § 6(b).

## INVENTION

The Appellant describes the invention at issue on appeal as follows.

> In accordance with the present invention, the address generation logic has a first address generation path and at least one further address generation path. The first address generation path is operable to determine the target address if the selected prefetched instruction is a first prefetched instruction in the plurality, i.e. that prefetched instruction within the plurality of prefetched instructions that appears first in the instruction stream. The at least one further address generation path is operable to determine the target address if the selected prefetched instruction is one of the other prefetched instructions in the plurality. The first address generation path is arranged to generate the target address more quickly than the at least one other address generation path, with the result that if the first prefetched instruction is the selected prefetched instruction, the prefetch unit is operable to output the associated target address as the fetch address one or more cycles earlier than if one of the other prefetched instructions is the selected prefetched instruction.

(Spec. 4.)

## ILLUSTRATIVE CLAIM

> 1. A data processing apparatus, comprising:
>
> a processor operable to execute a stream of instructions;
>
> a prefetch unit operable to prefetch instructions from a memory prior to sending those instructions to the processor for execution, the prefetch unit being operable to receive from the memory simultaneously a plurality of prefetched instructions from sequential addresses in memory, and being operable to detect whether any of those prefetched instructions are an instruction flow changing instruction, and based thereon to output a fetch address for a next instruction to be prefetched by the prefetch unit;

> address generation logic, within the prefetch unit and responsive to a selected prefetched instruction that is detected to be said instruction flow changing instruction, for determining a target address to be output as the fetch address, the address generation logic having a first address generation path for determining the target address if the selected prefetched instruction is a first prefetched instruction in said plurality, and at least one further address generation path for determining the target address if the selected prefetched instruction is one of the other prefetched instructions in said plurality, the first prefetched instruction being earlier in said stream than said other prefetched instructions, the first address generation path generating the target address more quickly than the at least one further address generation path; and
>
> a pipeline stage, provided in said at least one further address generation path, for increasing generation speed of the target address by the first address generation path, whereby, in the event that the first prefetched instruction is said selected prefetched instruction, the prefetch unit outputs the associated target address as the fetch address earlier than if one of said other prefetched instructions is said selected prefetched instruction.

## REJECTIONS

Claims 1-6, 10-16, 20, and 21 stand rejected under 35 U.S.C. § 103(a) as obvious over ARM System-on-Chip Architecture, 2000 ("Furber") and Computer Architecture - A Quantitative Approach ("Patterson").

Claims 7-9 and 17-19 stand rejected under § 103(a) as obvious over Furber; Patterson; and U.S. Patent 5,848,269 ("Hara").

## ISSUE

The Examiner admits that Furber "fails to teach: a pipeline stage, provided in said at least one further address generation path, for increasing

generation speed of the target address by the first address generation path." (Answer 5.) He finds, however, that "Patterson teaches that pipelining a processor, or adding stages of a pipeline, will reduce CPI [i.e., clock cycles per instruction], and reduce clock cycle time (increasing the rate at which the clock runs) (Page A-3), which would then speed up execution of the first address path, due to the increased clock rate." (*Id.*) The Appellant argues that "there is no specific structure (the claimed 'pipeline stage'), method step or logic meeting the limitations of Appellant's independent claims 1, 11 and 21, respectively." (Reply Br. 8.) Therefore, the issue before us is whether the Examiner has shown that the combination of Furber and Patterson would have suggested providing a pipeline stage in an address generation path for determining the target address of a selected prefetched instruction if the instruction is other than the first prefetched instructions in a plurality of prefetched instructions as required by independent claims 1, 11, and 21.

## FINDINGS OF FACT

Independent claims 1, 11, and 21 require a first address generation path for determining the target address of a selected prefetched instruction if the instruction is a first prefetched instruction in a plurality of prefetched instructions, at least one other address generation path for determining the target address if the selected prefetched instruction is one of the other prefetched instructions in the plurality of prefetched instructions, and a pipeline stage provided in the at least one further address generation path.

## ANALYSIS

Here, independent claims 1, 11, and 21 require a first address generation path, at least one other address generation path, and a pipeline stage provided *in the at least one further address generation path*. In contrast, the Examiner concludes that it would have been obvious to add stages of a pipeline as taught by Patterson *to a first address path*. (Answer 5.) Even is such an addition would have been obvious, however, the resultant combination still would not have suggested the claimed invention, i.e., *a pipeline stage in the at least one further address generation path*. The Examiner does not allege, let alone show, that the addition of Hara cures the aforementioned deficiency of Furber and Patterson.

## CONCLUSION

Based on the aforementioned facts and analysis, we conclude that the Examiner has not shown that the combination of Furber and Patterson would have suggested providing a pipeline stage in an address generation path for determining the target address of a selected prefetched instruction if the instruction is other than the first prefetched instructions in a plurality of prefetched instructions as required by independent claims 1, 11, and 21 or claims 2-10 and 12-20, which depend therefrom.

DECISION

We reverse the rejections of claims 1-21.

REVERSED

rwk

NIXON & VANDERHYE, PC
901 NORTH GLEBE ROAD, 11TH FLOOR
ARLINGTON VA 22203